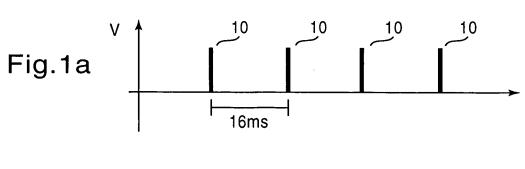
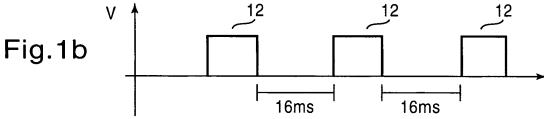
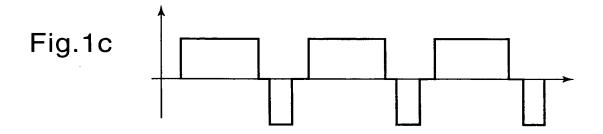
## **IN THE DRAWINGS**:

Replacement Figures 1-4 are included herewith to respond to an objection to the drawings made in the Office Action issued September 9, 2003. Applicants respectfully submits that the substitute figures comply with 37 C.F.R. §1.83 and find support from the specification of the instant application and the provisional application, 60/103,688, upon which the instant application claims priority from under 35 U.S.C. §119(e).







all is regardly processors



## Appl.No. 09/415,679 Relpy to Notice of Office Action of September 9, 2003 Replacement Sheet

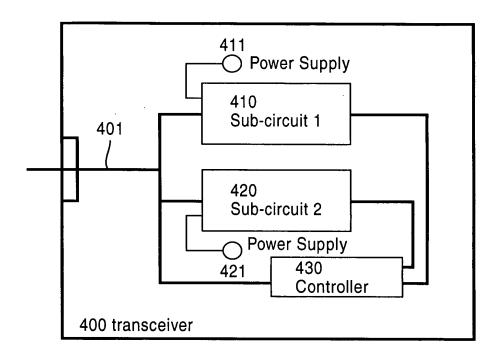
PCS: bypass: 100	OFF	OFF	띥	25	25	25	OFF
PCS bypass 10	20	20	OFF	OFF	20	OFF	OFF
Test	OFF	OFF	25	25	25	25(a)	OFF
FX:	OFF	OFF	25	25	25	25(a)	OFF
Serial 10 BT	20	20	OFF	OFF	10	10(a)	25
100 Base TX	OFF	OFF	25	25	25	25(a)	OFF
10 Base	20	20	OFF	OFF	2.5	2.5(a)	25
Auto- Neg	OFF	JJ0	OFF	340	25	OFF	25
Energy:	OFF.	OFF	OFF	OFF	25/2.5	얦	8
Power	냸	뜐	Ю	뜐	붠	생	병
Clock Name:	bt_txc_20	bt_rxc_20	tx_txc	tx_rxc	mii_txc	mii_rxc	cp_arb

Signal Name   Power   Energy Auto-	Power	Energy: Detect	Auto- Neg	Power Energy Auto- 10 Base   Down Detect Neg	100 Base TX	FX Mode	100 FX Test PCS Base TX Mode Loopback bypass 10	PCS bypass 10	PCS: bypass 100
mr_pd_pll	-	-	0	0	0	0	0	0	0
mr_pd_equal	-	_	0	1	0	1	0	-	0
mr_bt_revr		-	0	0	1	1	-	0	-
mr_pd_lp	-	_	0	•	1	1	1	-	
mr_pd_en_det	-	0	0	LINK	FINK	-	1	LINK(a)	LINK(b)
mr_pd_fx	-	+	-	-	-	0	0	1	-

Fig.2

-ig.3

Fig.4



SEVERY ON PRINCE